XUP Professor Workshop Invitation
DSP Design Flow Workshop
University of New Mexico

Dear University faculty member,

You are cordially invited to participate in the DSP Design Flow Professor workshop hosted by the Xilinx University Program and the University of New Mexico. The workshop is designed to provide University faculty members with introduction to the System Generator for DSP software through a series of lectures and hands on labs. The workshops are free of charge and will be held at the University of New Mexico in Albuquerque, NM from 9am – 5pm on Thursday, August 5 and Friday, August 6, 2004.

ACADEMIC DONATION
Each faculty member that attends the workshop will receive a donation of the following Xilinx Products:

- ISE Foundation FPGA development software (valued at $2,495.00)
- System Generator for DSP (valued at $1,995.00)
- Embedded Developers Kit (valued at $495.00)
- Forge (valued at $4,995.00)
- Chipscope-Pro (valued at $695.00)
- Choice of the following hardware platforms:
  - The new ML310 Virtex-II Pro based PCI development platform (valued at $2495.00)
  - Digilent D2SB-DIO4 (valued at $134.00)

ML310 Virtex-II Pro	**Digilent D2SB-DIO4**
Virtex-II Pro 2VP30 FPGA 256 MB DDR DIMM System ACE CF controller 512 MB CompactFlash card Onboard 10/100 Ethernet NIC 4 PCI slots (3.3V and 5V) LCD character display and cable FPGA serial port connection RS-232 mini-cable Personality module interface Standard JTAG connectivity ALi Super I/O – 1 parallel and 2 serial ports – 2 USB ports – 2 IDE connectors – GPIO – SMBus Interface – AC97 Audio CODEC – PS/2 keyboard and mouse ports	Spartan XC2S200E-200 FPGA with 200,000 gates and 200+MHz operation 43 available user I/O's routed to six 40-pin expansion connectors A socket for a JTAG-programmable 18V02 Flash ROM Dual on-board 1.5A power regulators (1.8V core and 3.3V I/O) A surface-mount 50MHz oscillator and a socket for a second oscillator A JTAG programming port and programming cable Status LED & pushbutton for basic I/O Four-digit seven-segment display 8 LEDs 8 Switches 4 debounced pushbuttons VGA Port 5V PS/2 Port

COURSE DESCRIPTION
The DSP Design Flow workshop provides an introduction to the advanced tools you need to design and implement DSP algorithms targeting FPGAs. This intermediate workshop in implementing DSP functions focuses on learning how to use System Generator for DSP, as well as HDL design flow, CORE Generator software, and design implementation tools. Through hands-on exercises, you will implement a design from algorithm concept to verification.

WHO SHOULD ATTEND?

University faculty involved in DSP related courses and research that want to understand how to implement a DSP design without being expert FPGA designers. Attendees will learn how certain decisions made up-front will impact the resulting implementation for a given algorithm.

PREREQUISITES

- Fundamentals of MATLAB/Simulink and Xilinx FPGAs
- Basic knowledge of VHDL
- Basics of digital signal processing theory for functions such as FIR (Finite Impulse Response) filters, oscillators and mixers, and FFT (Fast Fourier Transform) algorithms

SKILLS GAINED

After completing this training, attendees will be able to:

- Understand the strengths and weaknesses of three design flows (HDL, CORE Generator, System Generator)
- Make a decision regarding which design flow is more appropriate based on needs and FPGA expertise
- Understand the impact of some decisions made in the Simulink environment based on the resulting size of the FPGA design
- Debug and optimize a design in the Simulink environment
- Use advanced features of System Generator

WORKSHOP GOALS

- Learn how to implement a DSP design without having to be an FPGA expert
- Become comfortable using System Generator to develop lectures & labs, or implement research projects.

WORKSHOP AGENDA

Day 1: DSP Design Implementation Tools

- Agenda
- Introduction
- DSP Design Flows in FPGAs
- Lab 1: Creating a 12x8 MAC using VHDL
- Lab 2: Creating a 12x8 MAC using the Xilinx Core Generator
- Lab 3: Understanding the basics of System Generator through the construction of a MAC
- Digital Filtering
- Lab 4: Designing a FIR Filter Using the FDATool and FIR Blocks

Day 2: Digital Signal Processing Functions

- HDL Co-Simulation
- Lab 5: MAC FIR Filter Verification Using Co-Simulations
- Looking Under the Hood
- Lab 6: Looking Under the Hood
- Controlling the System
- Lab 7: Controlling the System
- Lab 8: Designing a MAC FIR

Wrap up

LAB DESCRIPTION

This lab-intensive class gives you hands-on experience using the System Generator for DSP to visualize, simulate, verify, and implement DSP algorithms in Xilinx FPGAs. The labs start at a descriptive level and

build upon each other. Students should expect each successive lesson's challenge to increase. Many new v6 System Generator for DSP features are identified.

TO REGISTER
University faculty may register online at the Xilinx University Program (http://university.xilinx.com) to attend the workshop. If you have not done so, please sign-up for access to receive a username/password. After you receive your username/password, you will be able to click on the **Professor Workshops** link to register for the workshop.

If you experience any difficulties, you may register by sending an email to xup@xilinx.com. Please include your contact information and answer the questions below, as follows:

- Email Title: Rice DSP Workshop
- Full Name:
- Title:
- University name and department:
- Address:
- City, State, Country, Postal Code
- Phone
- Email

1. Are you currently using programmable logic devices in your course work?
2. Have you ever attended an XUP workshop before?
3. What design entry tools are you familiar with?
4. Do you currently have Xilinx software?
5. Is there anything that you would like the workshop to cover which was not mentioned in the Course Contents description? If so, what is it?

TRAVEL & LODGING
Please refer to the following URL:
http://www.eece.unm.edu/xup/workshops.htm

Sincerely,

Xilinx University Program
xup@xilinx.com